REMARKS

By this amendment, claims 22-29, 33 and 34 have been amended and claims 35-37 have been added. Accordingly, claims 22-37 are currently pending in the application, of which claims 22 and 28 are independent claims. Applicant respectfully submits that the above amendments do not add new matter to the application and are fully supported by the specification. The Office Action indicates that claims 31-34 contain allowable subject matter.

In view of the above Amendments and the following Remarks, Applicant respectfully requests reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Rejections Under 35 U.S.C. §102

Claims 22-27 stand rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 5,737,049 issued to Shin, *et al.* ("Shin"). Applicant respectfully traverses this rejection for at least the following reasons.

As the specification clearly indicates, "an object of the present invention is to reduce the number of photolithograph steps ... the number of mask is reduced by etching a semiconductor layer, using the patterned [passivation] film as a mask." (Specification, page 4, lines 18-27).

For example, Fig. 7B of the present application shows the gate insulating layer 20, the amorphous silicon layer 30 and the n+ amorphous silicon layer 40 are formed sequentially without being patterned.

As shown in Fig. 7E, the amorphous silicon layer 30 remains the same even after the passivation layer 61 is deposited. After the passivation layer 61 is patterned, the exposed portion of the amorphous silicon layer 30 is removed by using the patterned passivation layer 61 as a

mask, as shown in Fig. 7F. Thus, according to the presented application, no photolithography step is required to pattern the amorphous silicon layer 30

Also, as shown in Fig. 7D, the n+ amorphous silicon layer 40 remains the same until the conductive layer is patterned to form the data line 51, source electrode 52 and drain electrode 53. After the conductive pattern is patterned, the exposed portion of the n+ amorphous silicon layer 40 is removed by using the data line 51, source electrode 52 and drain electrode 53 as a mask. Thus, no photolithography step is required to pattern the n+ amorphous silicon layer 40.

Contrarily, Fig. 2B of Shin shows the amorphous silicon layer 25, 27 and the n+ silicon layer 26, 28 being patterned before forming the source electrode 29 and the drain electrode 30. Thus, according to Shin, an extra photolithography step is performed to pattern the amorphous silicon layer 25, 27 and the n+ silicon layer 26, 28. As mentioned above, the present invention is directed to removing the photolithography step for patterning the source electrode 29 and the drain electrode 30. With this in mind, amended independent claim 22 recites:

> "22. A method for manufacturing a thin film transistor array panel, comprising steps of:
> forming a gate line and a gate electrode on a substrate by using *a first mask*;
> forming an insulation layer on the gate line and on the gate electrode;
> forming a semiconductor layer on the insulating layer;
> forming a data line, a source electrode and a drain electrode on the substrate by using *a second mask*;
> forming a passivation film on the semiconductor layer, the data line, the source electrode and the drain electrode by using *a third mask*, the passivation film exposing a portion of the drain electrode and a portion of the semiconductor layer;
> removing the exposed portion of the semiconductor layer; and
> forming a pixel electrode connected to the exposed portion of the drain electrode by using *a fourth mask*."

It should be noted that, according to the invention defined in claim 1, no mask is used to pattern the semiconductor layer. Contrarily, Shin requires at least five masks for the process steps shown in Fig. 2A to Fig. 2F.

Specifically speaking, in Fig. 2A, the first mask would be used to form the gate electrode pattern 21 and 22. In Fig. 2B, the second mask would be used to form the amorphous silicon layer pattern 25, 27 and the n+ silicon layer pattern 26, 28. In Fig. 2C, the third mask would be used to form the source and drain electrode pattern 29, 30. in Fig. 2E, the fourth mask would be used to form the passivation layer pattern 31. In Fig. 2F, the fifth mask would be used to form the pixel electrode pattern 33.

The claimed invention eliminates the photolithography step to form the amorphous silicon layer pattern 25, 27 and the n+ silicon layer pattern 26, 28 by the second mask. Thus, it is submitted that the claimed method is substantially different from the method disclosed in Shin. For this reason, it is submitted that claim 22 is patentable over Shin. Claims 23-27 are dependent from claim 22 and hence would be also patentable at least for the same reason.

Accordingly, Applicant respectfully requests withdrawal of the 35 U.S.C. §102(e) rejection of claims 22-27.

Rejections Under 35 U.S.C. §103

Claims 28-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable Shin. Applicant respectfully traverses this rejection for at least the following reasons.

Amended independent claim 28 recites:

"28. A method for manufacturing a thin film transistor array panel, comprising steps of:

depositing a first conductive layer on a substrate;

patterning the first conductive layer *by using a first mask* to form a gate line and a gate electrode;

depositing an insulating layer on the gate line and on the gate electrode;;

depositing a semiconductor layer on the insulating layer;

depositing a second conductive layer on the insulating layer;

patterning the second conductive layer *by using a second mask* to form a data line, a source electrode, and a drain electrode;

depositing a passivation layer on the semiconductor layer, the drain electrode, the source electrode and the data line;

patterning the passivation layer *by using a third mas*k to expose a portion of the semiconductor layer, a portion of the gate line, a portion of the data line, a portion of the insulating layer;

removing the exposed portion of the insulating layer; and

depositing a third conductive layer on the passivation layer and the insulating layer; and

patterning the third conductive layer to form a pixel electrode that contacts the exposed portion of the drain electrode *by using a fourth mask.*"

As previously mentioned, according to Shin, at least five masks are required for the process steps described in Figs. 2A to 2F. However, the processing steps of claim 28 requires only four masks because the mask for patterning the semiconductor layer has been eliminated.

No secondary reference has been introduced to conclude that it would have been obvious for an ordinary skilled person in the art would have been motivated to modify the processing steps of Shin such that the photolithography step for forming the amorphous silicon layer pattern 25, 27 and the n+ silicon layer pattern 26, 28 is eliminated.

For this reason, it is submitted that claim 28 is patentable over the cited references. Claims 29 and 30 are dependent from claim 28 and would be also patentable at least for the same

reason. Accordingly, Applicant respectfully requests withdrawal of the 35 U.S.C. §103(a) rejection of claims 28-30.

Other Matters

In addition to the aforementioned amendments made to claims 22 and 28, in this response, claims 22-29, 33 and 34 have been amended solely for better wording and clarification. Also, claims 35-37 have been newly added to further limit claim 34. These amendments are not made for the purpose of avoiding prior art or narrowing the claimed invention, and no change in claim scope is intended. Therefore Applicant does not intend to relinquish any subject matter by these amendments.

CONCLUSION

Applicant believes that a full and complete response has been made to the pending Office Action and respectfully submit that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicant respectfully submits that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicant's undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

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